REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the application. In previous responses, the Applicant canceled Claims 5, 12 and 19 without prejudice or disclaimer. In the present response, the Applicant has not amended, canceled, or added any claims. Accordingly, Claims 1-4, 6-11, 13-18 and 20 are currently pending in the application.

I. Rejection of Claims 1-4, 6, 8-11, 13, and 15-18 under 35 U.S.C. §103

The Examiner has rejected Claims 1-4, 6, 8-11, 13, and 15-18 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,631,912 to Mote (hereinafter "Mote") further in view of U.S. Patent No. 7,124,340 to Bos, *et al.* (hereinafter "Bos"). The Applicant respectfully disagrees since the cited portion of the cited combination of Mote and Bos do not teach or suggest port access circuitry on a integrated circuit (IC) that denies access to a memory of the IC when a testing port is disabled as recited in pending independent Claims 1, 8, and 15.

At item 7 at the middle of page 3 of the Office Action, the Examiner states that Mote discloses a system for denying access to a memory in an IC comprising:

> ...port access circuitry coupled to said testing port, that disables said testing port based on said configuration and denies access to said memory when said testing port is disabled (col. 4, lines 31-62, see also, col. 4, lines 17-30 and col. 6 lines 10-34).

The cited portions of Mote teach that "each of the output enable locations within the JTAG BSR are strung together (e.g., in adjacent locations within the JTAG boundary scan data shift register) so that the output enable bits used to control the impedance mode of the interfaces 128, 138, 148 can be shifted through in the minimum required time." (*See* lines 24-30 of column 4 of Mote.) The cited portions of Mote further teach that an IC has interfaces to separate PCI, µP, and memory busses. The

boundary scan registers for each of the interfaces are connected, or "strung together." (*See, e.g.*, the connections from element 205 to 210, element 210 to element 215, and element 215 to element 205 of Fig. 2 in Mote.) This allows for one of the interfaces of one of the three busses to be disabled while the other two interfaces to the other two busses remain enabled. As taught in the Abstract, *e.g.*, Mote teaches a "specially configured JTAG test circuit allows multiple bus connections within an integrated circuit to be selectively placed in a high impedance state in an efficient manner."

Thus, the cited portions of Mote teach disabling one bus from access to the IC while explicitly allowing access to the IC by two other busses. As such, the port access circuitry of Mote that disables a testing port does NOT deny access to a memory of the IC. On the contrary, as noted above, the cited portions of Mote teach port access circuitry that disables a testing port for one bus while explicitly allowing access to a memory of the IC through the other two bus interfaces. Not only do the cited portions of Mote not teach denying access to a memory when a testing port is disabled, the cite portions of Mote actually teach away from this limitation since access to the memory is explicitly taught via other bus interfaces. MPEP §2145 (X.)(D.)(2.) states:

> It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983).

Bos has not been cited to cure the above-noted deficiencies of Mote but to teach a testing port comprises a direct loopback between input and output pins thereof. (*See* Item 7, middle of page 3 of the Office Action.)

As such, the cited portions of the cited combination of Mote and Bos, as applied by the Examiner is, as established above, improper and does not provide a *prima facie* case of obviousness for pending independent Claims 1, 8, and 15. Accordingly, the Applicant respectfully requests the

Examiner to withdraw the §103(a) rejection of Claims 1-4, 6, 8-11, 13, and 15-18 and allow issuance thereof.

II. Rejection of Claims 7, 14, and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 7, 14 and 20 under 35 U.S.C. §103(a) as being unpatentable over Mote and further in view of Bos and U.S. Patent No. 6,522,100 to Hansford (hereinafter "Hansford"). As established above, the cited portions of the cited combination of Mote and Bos, as applied by the Examiner, do not provide a *prima facie* case of obviousness of pending independent Claims 1, 8, and 15. Hansford has not been cited to cure the above-noted deficiencies of the cited combination but to teach wherein the IC is a baseband chip of a mobile communication device. (*See* Item 18 at the middle of page 5 of the Office Action.) As such, the cited portions of the cited combination of Mote, Bos, and Hansford, as applied by the Examiner, do not establish a *prima facie* case of obviousness of pending independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 7, 14, and 20 and allow issuance thereof.

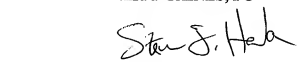
III. Conclusion

In view of the foregoing remarks, the Applicant sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-4, 6-11, 13-18, and 20.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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